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PATENT & TRADEMARK OFFICE

S/N 10/679,593

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Deshanand Singh et al.	Examiner: Tat, Binh C
Serial No.:	10/679,593	Group Art Unit: 2825
Filed:	October 6, 2003	Docket No.: ALT.P024 (A01002)
Title:	Method and Apparatus for Performing Layout-Driven Optimizations on Field Programmable Gate Arrays	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE TO REASONS FOR ALLOWANCE

Pursuant to 37 C.F.R. § 1.104, Applicants respectfully issue a statement commenting on the Examiner's reasons for allowance.

PAGE 4/5 * RCVD AT 8/13/2009 6:55:32 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/16 * DNIS:2732885 * CSID:2173567373 * DURATION (mm-ss):01-24